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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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GRAY, CARY, WARE & FREIDENRICH LLP
1221 SOUTH MOPAC EXPRESSWAY
SUITE 400
AUSTIN, TX 78746-6875

EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,594	BUCHT, THOMAS W.	
	Examiner	Art Unit	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The amendment filed February 4, 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows "logic associate with a register".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6, and 8-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The phrase "logic associated with a register"(see claim 1) and "register and associated logic" (see claim 8 and 13) was not previously disclosed in the specification at the time of the invention and thus constitutes as new matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,256,708 of Watanabe et al. referred hereinafter "Watanabe".

In regards to claim 1, Watanabe discloses:

directing logic associated with a register to drive data via a first device (see column 9 lines 53-63);

driving the data from the register to the first device and a second device simultaneously (see column 9 lines 53-63);

sampling the data and determining whether the data is valid, wherein the data is sampled and validity is determined by logic associated with the register. Watanabe discloses a valid flag corresponding of the data of address lower AD-2 of the A line, which represents the validity of the data (see column 9 lines 53-60); and

signaling the second device as to whether the data is valid or invalid. Watanabe discloses sending data to the cache memory when the data in the memory is invalid (see column 9 lines 53-63).

In regards to claim 2, Watanabe discloses:

the logic associated with the register is capable of analyzing at least one bit of the data to determine if the data is valid or invalid. Watanabe discloses a valid flag corresponding of the data of address lower AD-2 of the A line, implying the analyzing of the address lower AD-2 of the A line (see column 9 lines 53-63)

In regards to claim 3, Watanabe discloses:

the bit analyzed in determining the validity of the data is at least one of the most significant bit and a least significant. Watanabe discloses the AD-2 of the A line as the least significant it in the L2-TAGRAM and L2 status (see figure 3(b) and (c)).

In regards to claim 4, Watanabe discloses:

the first device comprises a CPU (see column 9 lines 59)

In regards to claim 5, Watanabe discloses:

wherein the second device comprises a memory device (see column 9 lines 62-63).

In regards to claim 6, Watanabe discloses:

wherein the memory device further comprises at least one of a content addressable memory, a hardware register, and a storage medium (see column 9 lines 62-63).

In regards to claim 7, Watanabe discloses:

a CPU in communication with and capable of directing a first hardware device see column 9 lines 53-63);

the first hardware device responsive to the CPU and capable of driving data pursuant to instructions from the CPU (see column 9 lines 53-63), wherein the hardware device is further capable of:

substantially simultaneously driving data to the CPU and a second hardware device (see column 9 lines 53-63);

analyzing one or more bits from the data driven by the first hardware device in determining validity of the data. Watanabe discloses a valid flag corresponding of the data of address lower AD-2 of the A line, which represents the validity of the data (see column 9 lines 53-60); and

transmitting a signal to the second hardware device regarding the validity of the data Watanabe discloses sending data to the cache memory when the data in the memory is invalid (see column 9 lines 53-63).

In regards to claim 8, Wanatabe discloses wherein first device comprises a hardware register (see figure 1 item 16).

In regards to claim 9, Wanatabe discloses wherein the second hardware device comprises writable hardware device (see column 9 lines 62-63).

In regards to claim 10, Wanatabe discloses wherein the writable hardware device comprises at least one of a content addressable memory, a hardware register, and a storage medium (see column 9 lines 62-63)

In regards to claim 11, Wanatabe discloses wherein the first hardware device analyze at least one of a most significant bit, and a least significant bit in determining the validity of the data. Watanabe discloses the AD-2 of the A line as the least significant it in the L2-TAGRAM and L2 status (see figure 3(b) and (c)).

In regards to claim 12, Wanatabe discloses wherein the validity signal is transmitted to the second hardware device at approximately near completion of the read cycle of the CPU (see column 9 lines 53-63).

Response to Arguments

Applicant's arguments filed February 4, 2004 have been fully considered but they are not deemed to be persuasive.

In regards to applicant's argument with respect to claim 1 on page 8 which cites: "...Consequently, the register and the associated logic of Watanabe simultaneously drive the data to a first device and to the register itself. In contrast, Claim 1 requires that the register and associated logic drive the data to a first device and a second device. Contrary to Watanabe, the second device is not identical to the register and its associated logic," examiner respectfully disagrees.

Watanabe discloses "... when the A line stored in the J stage in the inside of the L2S buffer 15 is to be transferred to the CPU 1 via a host bus 8, the L2S control section 12 cooperates with the L2 control section 11 to simultaneously perform processing of storing the A line into the L2 cache memory 200" (see column 9 lines 58-63 and fig 11). Thus, the L2 control section and L2S control section (logic associated with a register) transfers or drives A line (data) from a L2S buffer (register) to a CPU (first device) and a L2 cache memory (second device). Examiner maintains his rejection.

In regards to applicant's argument with respect to claim 1 on page 8 which cites: "Furthermore, Claim 1 recites that the register and associated logic sample the data and determine whether the data is valid. In contrast, Watanabe does not sample the data and

determine the validity of the data. While Watanabe may determine the status of cache memory which is being requested, this requires access to a separate status register (col 9 lines 64)," examiner respectfully disagrees.

Wanatabe discloses the VALID flag corresponds to the address lower AD-2 of line A line or data (see column 9 lines 53-56). Thus the A line (data) must be sampled to set the VALID flag to indicate "valid" or "invalid", which determines whether the data is valid. Examiner maintains his rejection.

In regards to applicant's argument with respect to claim 7 on page 9 which cites: "...Applicant points out that Watanabe does not analyze the driven data but instead accesses a status register pertaining to a memory location," examiner respectfully disagrees.

Wanatabe discloses the VALID flag corresponds to the address lower AD-2 of line A line or data (see column 9 lines 53-56). Thus the A line (data) must be analyzed to set the VALID flag to indicate "valid" or "invalid", which determines whether the data is valid. Examiner maintains his rejection.

Applicant's argument on page 9 with respect to 13 has been considered and is persuasive. The 102(e) rejection of Wanatabe has been withdrawn.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (703) 305-8012. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5631.

Emerson Puente
5/9/04

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100